What is Claimed is:

1. A subsystem comprising:

a master comprising a clock generator for generating a first clock signal and a second clock signal which have different frequencies from each other; and

a plurality of slaves for receiving command and address signals from the master and transmitting data signals to the master ,

wherein the first clock signal is used for the command and address signals , and the second clock signal is used for the data signals .

2. The subsystem according to claim 1, wherein the master transmits command and address signals into the corresponding slave only at a rising edge of the first clock signal .

3. The subsystem according to claim 1, wherein the master transmits command and address signals into the corresponding slave only at a falling edge of the first clock signal .

4. The subsystem according to claim 1, wherein the

master transmits command and address signals into the corresponding slave at the rising and falling edges of the first clock signal .

5. The subsystem according to claim 1, wherein the slave is one of a memory module, a receiver and an arithmetic logic unit (ALU).

6. The subsystem according to claim 1, wherein the frequency of the first clock signal is lower than that of the second clock signal.

7. The subsystem according to claim 1, wherein the clock generator is a clock synchronization means.

8. The subsystem according to claim 7, wherein the clock generator further comprises a divider for dividing the first clock signal to generate the second clock signal.

9. The subsystem according to claim 8, wherein the clock generator further comprises:

a first driver for driving the first clock signal; and

a second driver for driving the second clock signal.

10. The subsystem according to claim 7, wherein the clock synchronization means is a phase locked loop circuit.